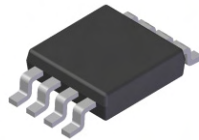


Features

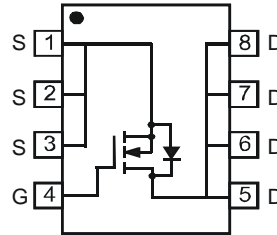
- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- **Lead Free By Design/RoHS Compliant (Note 1)**
- **"Green" Device (Note 2)**
- **Qualified to AEC-Q101 Standards for High Reliability**

Mechanical Data

- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram Below
- Weight: 0.072 grams (approximate)



Top View



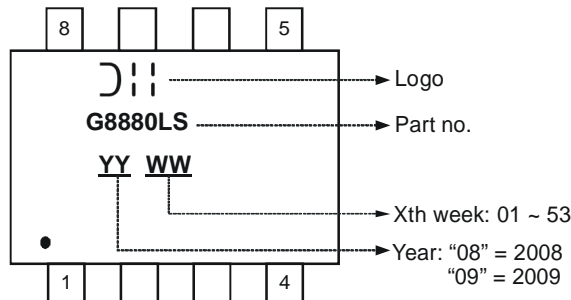
Top View
Internal Schematic

Ordering Information (Note 3)

Part Number	Case	Packaging
DMG8880LSS-13	SO-8	2500 / Tape & Reel

- Notes:
1. No purposefully added lead.
 2. Diodes Inc.'s "Green" policy can be found on our website at <http://www.diodes.com>.
 3. For packaging details, go to our website at <http://www.diodes.com>.

Marking Information



Maximum Ratings @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	30	V
Gate-Source Voltage			V_{GSS}	± 20	V
Continuous Drain Current (Note 4)	Steady State	$T_A = 25^\circ\text{C}$	I_D	11.6	A
		$T_A = 70^\circ\text{C}$		8.5	
Pulsed Drain Current (Note 5)			I_{DM}	80	A

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Power Dissipation (Note 4)	P_D	1.43	W
Thermal Resistance, Junction to Ambient @ $T_A = 25^\circ\text{C}$ (Note 4)	$R_{\theta JA}$	87	$^\circ\text{C/W}$
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

Electrical Characteristics @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 6)						
Drain-Source Breakdown Voltage	BV_{DSS}	30	-	-	V	$V_{GS} = 0V, I_D = 250\mu\text{A}$
Zero Gate Voltage Drain Current $T_J = 25^\circ\text{C}$	I_{DSS}	-	-	1.0	μA	$V_{DS} = 30V, V_{GS} = 0V$
Gate-Source Leakage	I_{GSS}	-	-	± 100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
ON CHARACTERISTICS (Note 6)						
Gate Threshold Voltage	$V_{GS(th)}$	1.0	1.5	2.0	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(on)}$	-	7.0	10	m Ω	$V_{GS} = 10V, I_D = 11.6A$
			9.6	14		$V_{GS} = 4.5V, I_D = 10.7A$
Diode Forward Voltage	V_{SD}	-	0.7	1.0	V	$V_{GS} = 0V, I_S = 2.1A$
DYNAMIC CHARACTERISTICS (Note 7)						
Input Capacitance	C_{iss}	-	1289	-	pF	$V_{DS} = 15V, V_{GS} = 0V,$ $f = 1.0\text{MHz}$
Output Capacitance	C_{oss}	-	187	-	pF	
Reverse Transfer Capacitance	C_{rss}	-	162	-	pF	
Gate Resistance	R_g	-	0.97	-	Ω	$V_{DS} = 0V, V_{GS} = 0V, f = 1\text{MHz}$
Total Gate Charge at 10V	Q_g	-	27.6	-	nC	$V_{GS} = 10V, V_{DS} = 15V,$ $I_D = 11.6A, I_G = 1.0\text{mA}$
Total Gate Charge at 5V	Q_g	-	14.4	-	nC	$V_{GS} = 5V, V_{DS} = 15V,$ $I_D = 11.6A, I_G = 1.0\text{mA}$
Gate-Source Charge	Q_{gs}	-	3.6	-	nC	
Gate-Drain Charge	Q_{gd}	-	4.9	-	nC	
Turn-On Delay Time	$t_{D(on)}$	-	7.04	-	ns	$V_{DD} = 15V, V_{GS} = 10V,$ $R_{GS} = 11\Omega, I_D = 11.6A$
Turn-On Rise Time	t_r	-	17.52	-	ns	
Turn-Off Delay Time	$t_{D(off)}$	-	36.13	-	ns	
Turn-Off Fall Time	t_f	-	19.67	-	ns	

- Notes:
- Device mounted on FR-4 PCB, with minimum recommended pad layout.
 - Repetitive rating, pulse width limited by junction temperature.
 - Short duration pulse test used to minimize self-heating effect.
 - Guaranteed by design. Not subject to production testing.

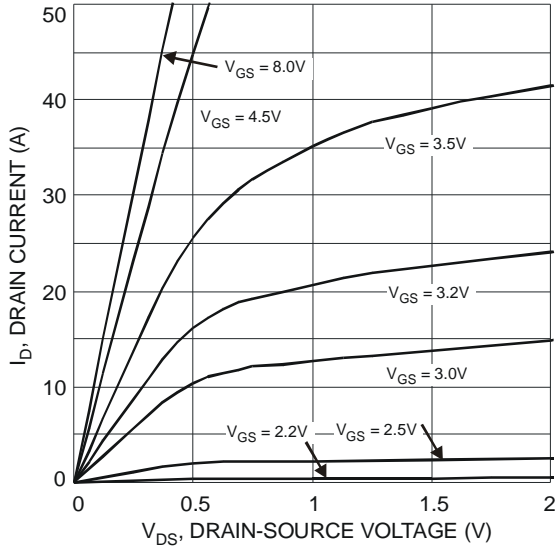


Fig. 1 Typical Output Characteristic

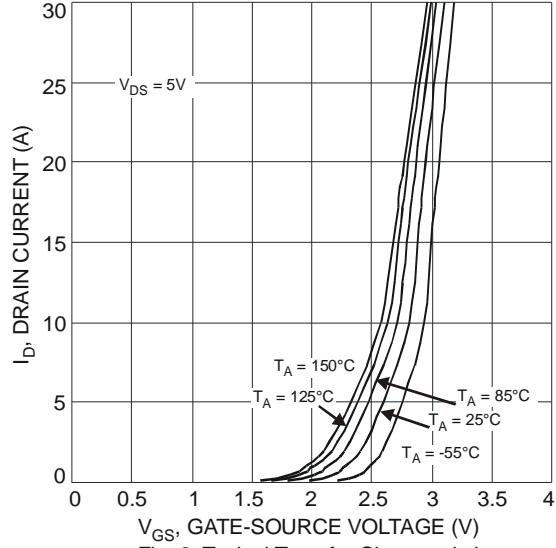


Fig. 2 Typical Transfer Characteristic

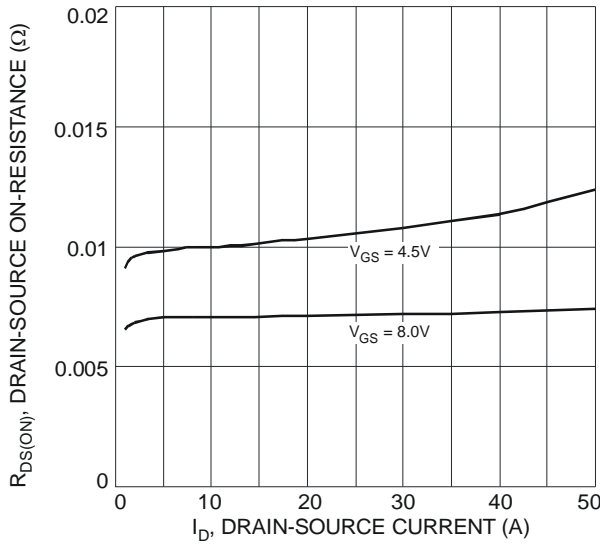


Fig. 3 Typical On-Resistance vs. Drain Current and Gate Voltage

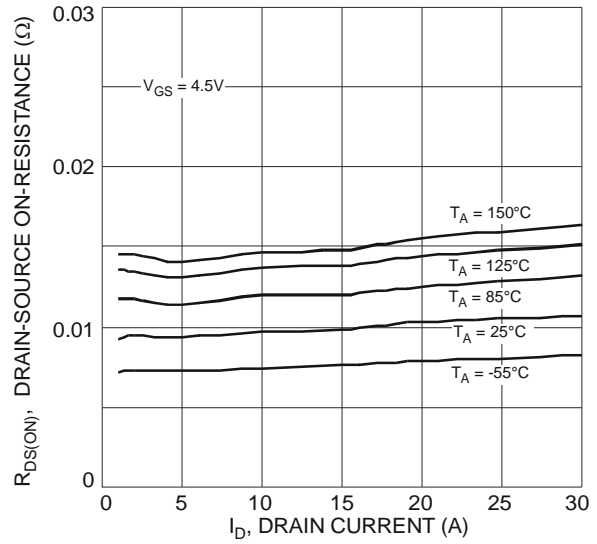


Fig. 4 Typical On-Resistance vs. Drain Current and Temperature

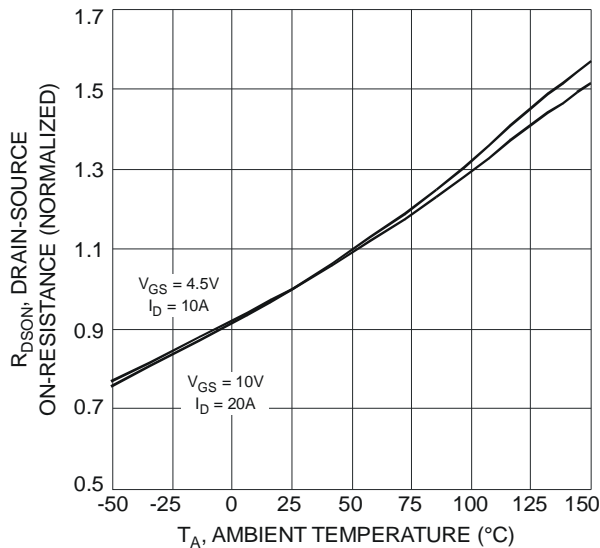


Fig. 5 On-Resistance Variation with Temperature

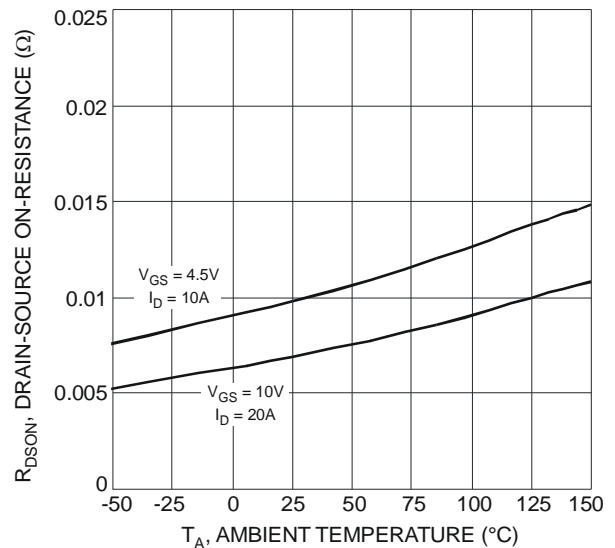


Fig. 6 On-Resistance Variation with Temperature

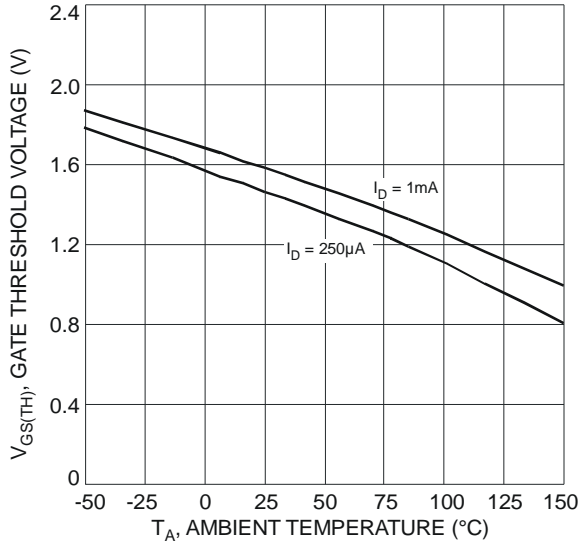


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

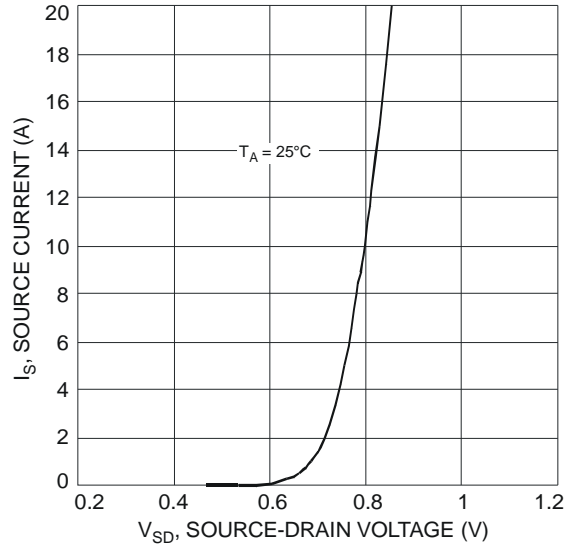


Fig. 8 Diode Forward Voltage vs. Current

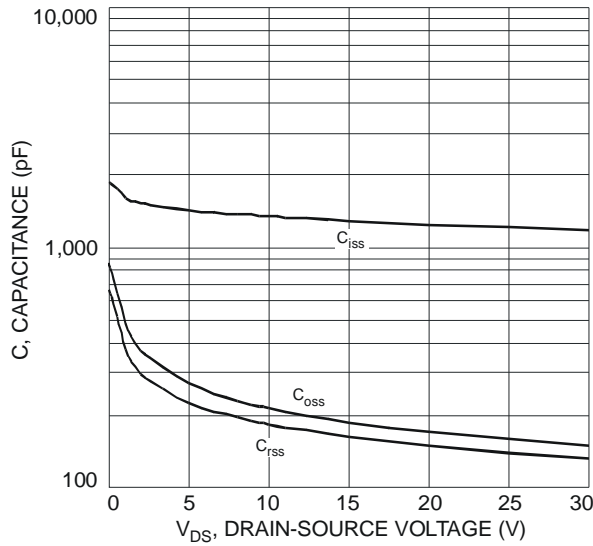


Fig. 9 Typical Total Capacitance

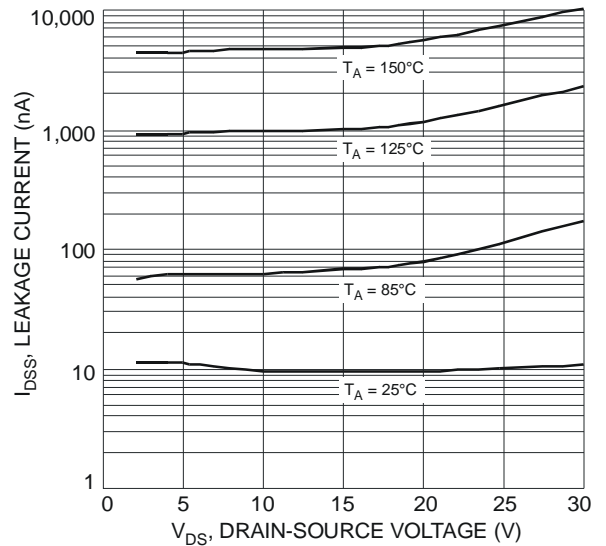


Fig. 10 Typical Leakage Current vs. Drain-Source Voltage

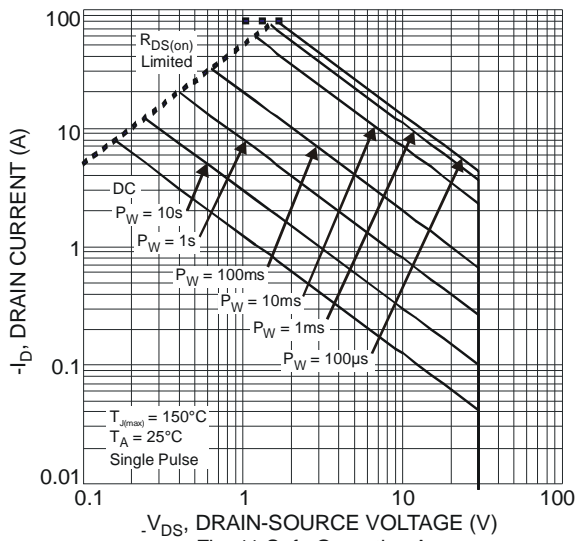


Fig. 11 Safe Operation Area

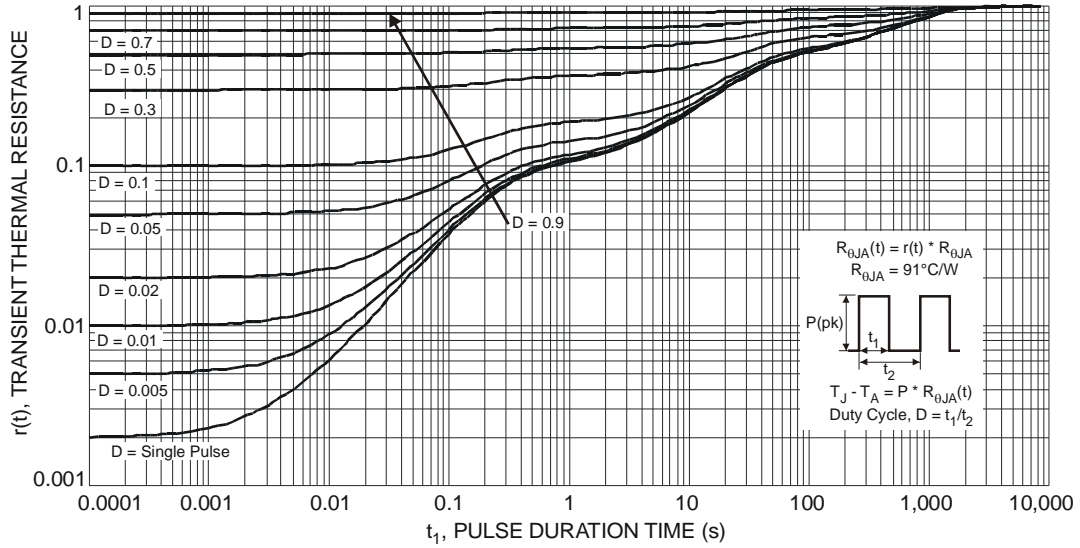
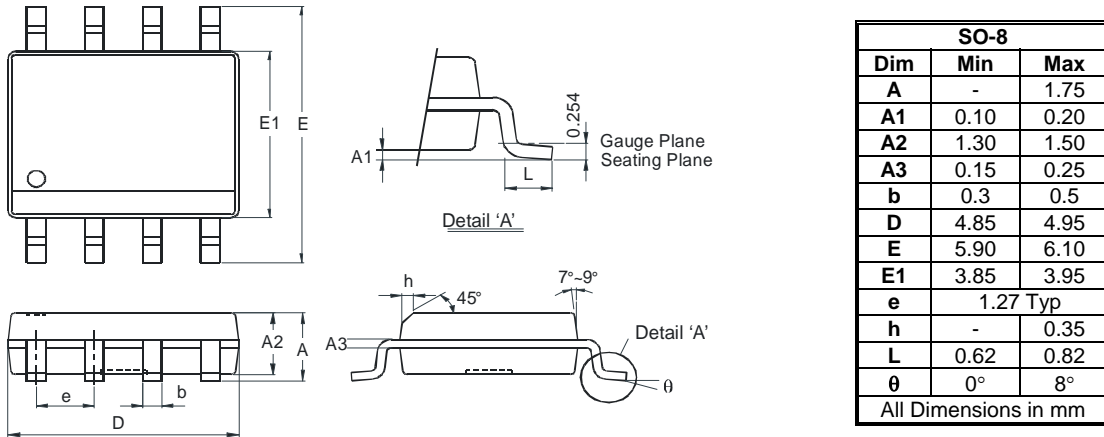
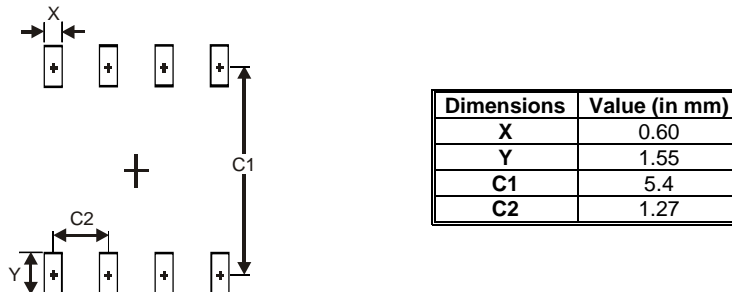


Fig. 12 Transient Thermal Response

Package Outline Dimensions



Suggested Pad Layout



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